IN THE SPECIFICATION

On page 6, please amend the paragraph starting at line 19 through line 4 of page 7 to read as follows:

B1

As defined within the Intel architecture instruction set, an exemplary macro-instruction 100 may comprise instruction prefixes 102 (each instruction prefix 102 being 0-4 bytes in length), an opcode 104 (1-2 bytes in length), a ModR/M operand indicator 106 (0-1 byte in length), an SIB of 108 (0-1 lengths in byte), address displacement 110 (0, 1 or 4 bytes in length), and an intermediate data constant 112 (0, 1 or 4 bytes in length). Opcode 104 may be either one or two bytes in length. For two-byte opcodes, the first byte is 0F.

On page 10, please amend the paragraph starting at line 5 through line 13 to read as follows:

B2

In the second pipe stage, instruction length decoder (ILD) 308 determines the length of the current instruction. IA instructions are variable length instructions varying in length from 1 to 15 bytes with prefixes and 1 to 11 bytes without prefixes. In order to properly align and decode the instructions, the length of the instruction must be determined. The bytes that are received from the ALN 306 stage are assumed to start with the first byte of instruction. The ILD 308 decodes these instruction bytes, determines the length of the instruction, and sends the length to the ALN 306 for subsequent instruction realignment and to a decode stage for marking the instruction boundaries.

On page 12, please amend the paragraph starting at line 8 through page 13, line 2 to read as follows:

B3

Figure 5 is a block diagram showing architecture details of ALN 306 and LEN 402. Data stream bytes are received into two 10x16-byte buffers 304 from MIQ buffers 302. The data stream is rotated into rotator 504. In one embodiment, rotator 504 consists of 12 bytes. Rotator 504 rotates the data bytes of two instructions. In one embodiment, an instruction has a maximum length of 11 bytes (without prefixes). If 12 bytes captures both instructions, then ALN 306 will have a maximum throughput. Rotator 504 is one pipe stage behind the decoding of the current instruction. Using the length vector obtained from the LEN 402, ALN 306 next shifts the current instruction into shifter 506. Shifter 506 shifts to the exact instruction start based on the length of the first instruction in the data stream. If rotator 504 does not contain the entire instruction required by shifter 506, rotator 504 rotates instruction data from buffers 304. Shifter 506 output gives the current instruction for the current pipe stage. It is assumed that the first instruction within the data stream begins at the beginning of the data buffer. Thus, during the current pipe stage, rotator 504 is obtaining instruction data for the current instruction while shifter 506 is obtaining data for the next instruction in the data stream.

On page 14, please amend the paragraph starting at line 3 through line 13 to read as follows:

B4 was A01

Initially, rotator 504 contains bytes 2-13 as shown in Table 2 for time 1. The shifter 506 contains bytes 2-13 and length is 0. LEN 402 determines the length of A. The length of A is returned to shifter 506. At time 2, shifter 506, using the length of A of 5 bytes, shifts bytes from rotator 504 into shifter 506 offset by the length of A and shifts A to LEN length decode unit (LD) 508. Thus, rotator 504 contains bytes 2-13, the shifter 506 now contains bytes 7-13, and LEN 402 contains bytes 2-6 (instruction A). Shifter 506 then shifts bytes 7-13 to LEN 402 for length determination of instruction B. At time

3, shifter 506, using the length of B of 3 bytes, shifts instruction B into LEN 402, bytes 10-18 are shifted into shifter 506, and rotator contains bytes 7-18. The process is repeated in order to shift instruction C into LEN 402 as shown in Table 2.

On page 16, please amend the paragraph starting at line 1 through line 10 to read as follows:

Figure 7 is a block diagram showing architectural details of one embodiment of the length decode unit (LD) 508. LD 508 determines the length of various portions of the instruction received from ALN 306. ALN 306 shifts the current instruction from the shifter 506 onto the LD 508. Within the [LD] 508, opcode-plus-immediate logic unit OPIMM 602 determines the length of the opcode 104 and immediate data 112 of the current instruction. B0 and B1 are inputs to OPIMM 602 together with the operand-size (Osz) signal. The Osz signal selects the sizes of operands that instructions operate on. When the 16-bit Osz signal is in force, operands may be either 8 or 16 bits. When the 32-bit Osz signal is in force, operands may be 8 or 32 bits.

On page 18, please amend the paragraph starting at line 9 through line 14 to read as follows:

Table 3 shows the possible outputs from OPIMM 602. The outputs are dependent on whether the opcode 104 is one or two bytes and the possible lengths of the immediate data 112. The immediate data may be 1, 2, 4 or 6 bytes in length. Thus, the opcode plus immediate may be 1, 2, or 6 bytes in length. Table 3 indicates the possible combinations of opcode and immediate displacement.